WHAT IS CLAIMED IS:

1. A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a semiconductor substrate;

a series of N epitaxial layers, an initial layer of the series being on, and having a lattice mismatched with, a lattice of the substrate, each higher layer being on a previous layer, an Nth layer being an uppermost layer of the series;

an isolation trench having rounded corners formed in the uppermost Nth layer of the series;

an insulative material filling the isolation trench; and

a selective top epitaxial layer on the uppermost Nth layer of the series.

2. A semiconductor structure as in Claim 1, wherein each layer of the series has an equal or higher lattice mismatch relative to the lattice of the substrate than the lattice of the previous layer and the lattice of the top layer being mismatched with the lattice of the Nth layer of the series.

3. A semiconductor structure as in Claim 1, wherein upper and lower corners of the trench are rounded.

4. A semiconductor structure as in Claim 1, wherein upper corners of the trench are rounded.

5. A semiconductor structure as in Claim 4, wherein the radii of the corners are from about 5 to about 50 nm.

6. A semiconductor structure as in Claim 1, wherein the trench has a depth of less than about 6,000 Å.

7. A semiconductor structure as in Claim 1, wherein the rounded corners are formed by heating the Nth layer in a gaseous ambient.

8. A semiconductor structure as in Claim 7, wherein heating of the Nth layer is effected at a temperature within the range of about 700 C to about 950 C.

9. A semiconductor structure as in Claim 7, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

10. A semiconductor structure as in Claim 7, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

11. A semiconductor structure as in Claim 1, wherein the insulative material comprises silicon oxide.

12. A semiconductor structure as in Claim 1, wherein the top layer is less than about 250 Å thick.

13. A semiconductor structure as in Claim 1, wherein the series of N layers and the top layer are selected from the group consisting of: Si, Ge, C, a compound semiconductor, and combinations thereof.

14. A semiconductor structure as in Claim 1, wherein the series of N layers and the top layer comprise Si and Ge.

15. A semiconductor structure as in Claim 1, wherein a free surface of one or more of the layers is planarized before a next superjacent layer is present thereon.

16. A semiconductor structure as in Claim 15, wherein planarization is effected by CMP.

17. A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a semiconductor substrate;

a first epitaxial layer on the substrate;

a second epitaxial layer on the first layer;

an isolation trench having rounded corners formed in the second layer;

an insulative material filling the isolation trench; and

a selective top epitaxial layer on the second layer.

18. A semiconductor structure as in Claim 17, wherein the rounded corners are formed by heating the second layer in a gaseous ambient.

19. A semiconductor structure as in Claim 18, wherein heating is effected at a temperature within the range of about 700 C to about 950 C.

20. A semiconductor structure as in Claim 18, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

21. A semiconductor structure as in Claim 18, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

22. A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a semiconductor substrate;

a first crystalline epitaxial layer on the substrate;

a second crystalline layer on the first layer;

a trench formed in the second layer; and

a top epitaxial layer on the second layer.

23. A semiconductor structure as in Claim 22, wherein upper and lower corners of the trench are rounded.

24. A semiconductor structure as in Claim 22 wherein upper corners of the trench are rounded.

25. A semiconductor structure as in Claim 23, wherein the radii of the corners are from about 5 to about 50 nm.

26. A semiconductor structure as in Claim 22, wherein the trench has a depth of about 6,000 Å or less.

27. A semiconductor structure as in Claim 23, wherein the rounded corners are formed by heating the second layer in a gaseous ambient.

28. A semiconductor structure as in Claim 27, wherein heating is effected at a temperature within the range of about 700 C to about 950 C.

29. A semiconductor structure as in Claim 27, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

30. A semiconductor structure as in Claim 27, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

31. A semiconductor structure as in Claim 22, wherein the trench contains an insulative material comprising silicon oxide.

32. A semiconductor structure as in Claim 22, wherein the top layer is less than about 250 Å thick.

33. A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si, Ge, C, or a compound semiconductor.

34. A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si and Ge.

35. A semiconductor structure as in Claim 22, wherein

a lattice of a material of the first layer is mismatched with a lattice of the substrate; and

a lattice of a material of the second layer is mismatched with the lattice of the first layer.

36. A semiconductor structure as in Claim 35, wherein a lattice of a material of the top layer is mismatched with the lattice of the second layer.

37. A semiconductor structure as in Claim 22, wherein a free surface of one or more of the layers is planarized before a next superjacent layer is present thereon.

38. A semiconductor structure as in Claim 37, wherein planarization is effected by CMP.

39. A semiconductor structure usable for the fabrication of a strained channel transistor, comprising:

a silicon semiconductor substrate;

a first epitaxial layer of Si, Ge, C or a compound semiconductor on the substrate;

a second epitaxial layer of Si, Ge, C or a compound semiconductor on a planarized free surface of the first layer, a crystalline lattice of the second layer being mismatched with a crystalline lattice of the first layer;

an isolation trench having rounded corners formed in the second layer, the rounded corners being formed by annealing the second layer after trench formation at a temperature of about 700 C to about 950 C in a gaseous ambient containing O, H, N, He, Ne, Ar, Xe or a combination of two or more thereof, at a pressure of about 10 to about 1,000 Torr, the trench having a depth of less than about 6,000 Å, the corners having radii in the range of about 5 to about 50 nm;

insulative silicon oxide filling the isolation trench; and

a top selective epitaxial layer of Si, Ge, C or a compound semiconductor having a thickness of less than about 250 Å on a planarized free surface of the second layer, the crystalline lattice of the top layer being mismatched with the lattice of the second layer by an equal or greater amount than the mismatch between the first and second layers.

40. A structure as in Claim 39, wherein the top layer is unfaceted, the facing sides of the top layer and the silicon oxide engaging, or is faceted, a gap being present between the facing sides of the top layer and the silicon oxide.

41. A semiconductor structure usable in the fabrication of a strained channel transistor, comprising:

a semiconductor substrate;

a first crystalline epitaxial layer on the free surface of the substrate, a free surface of the first layer being planarized;

a second crystalline epitaxial layer on the planarized free surface of the first layer;

an isolation trench in the second layer;

an insulative material filling the trench; and

a selective epitaxial crystalline top layer on the free surface of the second layer.

42. A semiconductor structure as in Claim 41, wherein the top layer is faceted or unfaceted.

43. A semiconductor structure as in Claim 41, wherein the top layer is less than about 250 Å thick.

44. A semiconductor structure as in Claim 41, wherein the first, second and top layers comprise Si, Ge, C, or a compound semiconductor.

45. A semiconductor structure as in Claim 41, wherein the first, second and top layers comprise Si, Ge, or SiGe.

46. A semiconductor structure as in Claim 41, wherein

a material lattice of the first layer is mismatched with a lattice of the substrate; and

a material lattice of the second layer is mismatched with the lattice of the first layer.

47. A semiconductor structure as in Claim 46, wherein a material lattice of the top layer is mismatched with the lattice of the second layer.

48. A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a silicon semiconductor substrate;

a series of N epitaxial layers comprising Si, Ge, C or a compound semiconductor, the initial layer of the series being on the substrate and having a lattice mismatched with the lattice of the substrate, each of the higher layers of the series having a lattice mismatch with the substrate that is no less than that between (i) the initial layer and the substrate and (ii) the immediately underlying layer and the layer on which the immediately underlying layer resides, the Nth layer being the uppermost layer of the series, N being equal to or greater than 1;

an isolation trench less than about 6,000 Å deep having rounded corners formed in the Nth layer by heating the Nth layer after trench formation at a temperature of about 700 C to about 950 C in a gaseous ambient containing O, H, N, He, Ne, Ar, Xe or a combination of two or more thereof at a pressure of about 10 to about 1,000 Torr, the trench having a depth of less than about 6,000 Å and the corners having radii in the range of about 5 to about 50 nm;

an insulative Si-containing material filling the isolation trench; and

a top selective epitaxial layer of Si, Ge, C or a compound semiconductor having a thickness of less than about 250 Å on a free surface of the Nth layer, the crystalline lattice of the top layer being mismatched with the lattice of the Nth layer by an amount no less than the mismatch between the Nth layer and the (N-1)th layer.

49. A method of making a semiconductor structure from which a strained channel transistor may be fabricated, which comprises:

depositing a series of N epitaxial layers, the initial layer of the series being on a semiconductor substrate and each higher layer being on the previous layer, the Nth layer being the uppermost layer of the series, each layer of the series having equal or higher mismatch with the lattice of the substrate than the previous layer;

forming a trench having rounded corners in the Nth layer;

filling the trench with an insulative material; and

depositing a selective epitaxial top layer on the Nth layer, the top layer having equal or higher mismatch with the lattice of the substrate than the Nth layer.

50. A method as in Claim 49, wherein at least one of the layers of the series is planarized before deposition of the immediately higher layer.

51. A method as in Claim 49, wherein at least one of the layers of the series is annealed before deposition of the immediately higher layer.

52. A method as in Claim 51, wherein annealing is effected by heating to a temperature that is more than about 100 C greater than the temperature at which the layer is deposited in an atmosphere of H, N, He, Ne, Ar, Xe or a mixture of two or more thereof, at a pressure of about 10 to about 1,000 Torr.

53. A method as in Claim 49, wherein the layers of the series and the top layer are deposited at temperatures within the range of about 450 C to 950 C with a forming gas of SiH_4, Si_2H_6, SiH_2Cl_2,

GeH_4, Ge_2H_6, H, N, HCl, He, PH_3 or B_2H_6 containing Si, Ge, H, He, P, B, or As, at a pressure of less than about 100 mTorr.

54. A method as in Claim 49, wherein the corners of the trench are rounded by heating the top layer after trench formation to a temperature within a range of about 500 C to about 1,150 C in a gaseous ambient containing O, H, N, He, Ar, Xe, or a mixture of two or more thereof at a pressure within the range of about 10 to about 1000 Torr.

55. A method as in Claim 49, wherein the top layer is deposited by selective epitaxy to a thickness of about 250 Å or less.

56. A method as in Claim 49, wherein the trench filling step is effected before the deposition of the top layer is effected.

57. A method as in Claim 49, wherein the Nth layer is planarized prior to deposition of the top layer.

58. A method as in Claim 49, wherein the trench filling step is effected after the deposition of the top layer is effected.

59. A method as in Claim 49, wherein the Nth layer and the material filling the trench are planarized prior to deposition of the top layer.